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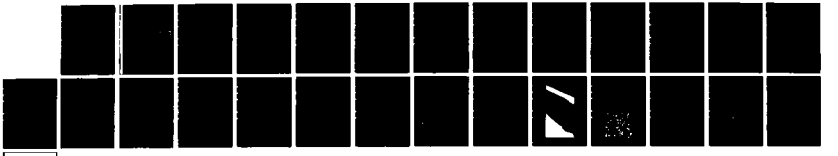

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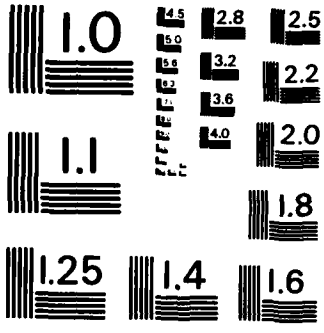

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NOVEL TECHNIQUES FOR THE FABRICATING AND CHARACTERIZATION OF GaAs MIS STRUCTURES

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Organometallic chemical vapor deposition (OMCVD) of Al_2O_3 on GaAs has been investigated as a means of fabricating metal-insulator-semiconductor field effect transistors (MISFET). Deposition at temperatures less than 400°C forms high-quality films of $-Al_2O_3$. Diffusion can alter the composition during high-temperature anneals. In-situ etching of the GaAs just prior to depositing the Al_2O_3 markedly reduced surface generation velocities, but inversion at the interface was not conclusively demonstrated.

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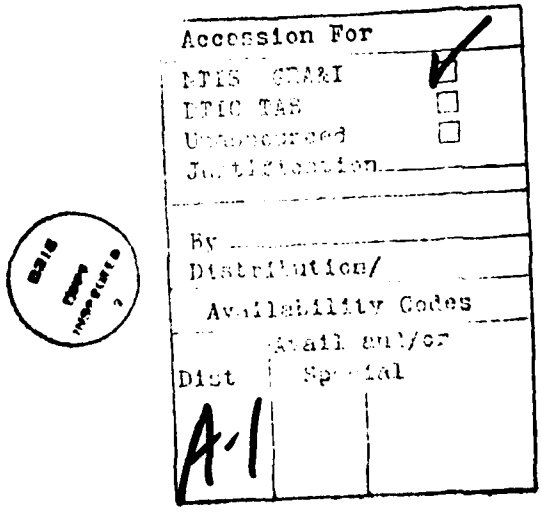

INTRODUCTION

This report describes the results obtained during the past year of the program initiated to develop the technology required for inversion of the surface of p-type GaAs.

We believe that the realization of inversion at the interface of a GaAs MIS structure is dependent upon starting with a substrate surface which is clean and free of damage, and subsequently depositing a high-quality insulator without the introduction of any interface perturbations during the deposition process. We suggested that the substrate surface requirements might be achieved by proper wet chemical etching followed by *in-situ* etching prior to insulator deposition, and that perturbations normally introduced during insulator deposition could be minimized or eliminated by employing a low temperature deposition process.

We chose to deposit the dieletric by the oxidation of organometallic compounds since this method permits high-quality film growth at the lowest possible temperatures (<400°C). An organometallic chemical vapor deposition system (OMCVD) which has the unique capability of *in-situ* etching was constructed for this purpose. We selected Al_2O_3 as the first insulator to investigate because of its close thermal expansion match to GaAs. In 1966 a paper was published which indicated that Al_2O_3 might be employed as the dielectric of a functional GaAs MIS structure (1). In that paper, the authors first deposited a layer of Al_2O_3 by the decomposition of aluminum-iso-propoxide followed by a layer of SiO_2. The SiO_2 layer was required because of an instability observed by the authors when only Al_2O_3 was used. In that paper, lateral MISFETs were fabricated and used to evaluate the inversion layer formation. This provided conclusive evidence of low interface state density between Al_2O_3 and p-type GaAs surfaces. The drawback of this approach was the relatively inferior quality of the Al_2O_3 films and the relatively high deposition temperatures (2). Our OMCVD approach addressed these problems.

The results of the development of the OMCVD and HCl *in-situ* etch process are presented in this report along with additional results obtained from investigations we felt were technically advantageous to the program.

The final goal of realizing inversion at the Al_2O_3/GaAs interface was not achieved. However, we feel that the results of this work indicate a direction for future investigations. These altenatives are presented.

I. Al_2O_3 Deposition and Characterization

A process has been developed for the deposition of Al_2O_3 films by the oxidation of trimethylaluminum (3). Process parameters have been evaluated and optimized to obtain reasonable growth rates and high-quality films at deposition temperatures as low as 300°C. The dependency observed for the growth rate on the oxygen concentration and the substrate temperature are shown in Figures 1 and 2.

The variation of TMAl flow resulted in changes of the deposition area (with a uniform growth region within this area) instead of an expected change in growth rate with uniform deposition. This phenonenon is shown in Figure 3 where the diameter of the uniform deposition area is plotted as a function of the TMAl(Ar) flow rate. The general thickness variations within this diameter are shown for several flow rates in the insert. The arrow in the insert shows the location of the funnel. For constant deposition times, as the flow is increased, the thickness in the uniform deposition region remains constant and the diameter increases. Based upon the data shown in Figure 2 we believe that the deposition rate in the uniform thickness region is kinetically limited. As the reactants flow towards the edges of the

wafer the TMAl concentration is diluted and the reaction becomes mass flow controlled. This results in a reduction of the growth rate as the perimeter of the deposition region is approached. When the flow is increased, the higher flux can support a kinetically controlled reaction over more of the substrate area before it is diluted to the level at which the reaction becomes mass flow controlled. This results in the observed increase in area.

The structural analyses of deposited Al_2O_3 films by TEM and low-angle x-ray diffraction show that some films are amorphous while, in others, the polycrystalline γ-Al_2O_3 phase dominates. This γ-phase is more predominant with films deposited at the higher deposition temperature provided oxygen flow rates during the deposition are greater than 30 cc/min. Amorphous films are evident at all deposition temperatures when oxygen concentrations (flow rates) are lower.

The index of refraction is plotted as a function of temperature in Figure 4. A progressive increase in the refractive index is observed with increasing deposition temperatures. The higher index of refraction with increasing deposition temperature is probably due to a corresponding change in the microstructure of the films from the amorphous to the polycrystalline γ-phase which was observed in the structural analysis. The index is significantly lower than that reported for σ and γ-Al_2O_3. However, the index for films deposited near 370°C compares very favorably with those reported for other higher temperature CVD deposition processes (2).

The dielectric constant, dielectric strength, and resistivity of films deposited at various temperatures and with various oxygen concentrations have also been measured. No trend was observed as a function of these parameters. The value of the dielectric constant varied between 7.5 and 7.8 while values of the dielectric strength ranged from 7.5 to 7.9×10^6 V/cm. The resistivity was greater than 10^{15} ohm-cm. As is the case with the index of refraction, these results compare favorably with those reported in the literature for Al_2O_3 films deposited by other techniques at higher temperatures.

The in-depth distribution of impurities in the Al_2O_3 film has been determined by secondary ion mass spectrometry. Impurities present in the films were initially identified by recording mass/charge spectra from 1 to 100. A typical in-depth profile is shown in Figure 5. The Al_2O_3 is deposited on a Si substrate. The carbon impurity, presumably from the organometallic, is probably inherent in this CVD process. However, the source of the Na impurity was initially less obvious. The $^{23}Na^+$ was detected above the background level at the film substrate interface and progressively increased as the surface was approached. This suggested the possibility of a temperature-dependent source which might be an integral part of the reactor. Accordingly, all pyrex glass parts of the reaction chamber were replaced with high purity quartz. No $^{23}Na^+$ could be detected in the Al_2O_3 films after this change was introduced.

II. Characterization Techniques

A process was developed for the fabrication of MIS test devices. This involved the development of a method for the application of good ohmic contacts to the rear surface of the relatively low concentration (1E16) p-type GaAs. We have found that a multilayer Au/Zn/Au (2000Å/4000Å/6000Å) vacuum deposition followed by a 400°C anneal for five minutes in Ar provides ohmic contacts which are satifactory for the MIS structure. A vacuum evaporation of of .010-.020 in. dia. Al dots were employed for the metal electrode. A computer- controlled capacitance/conductance measurement system was assembled for characterization of the MIS devices at 1 MHz and a manual system was assembled for measurements at frequencies between 20 Hz and 210 kHz. Software was generated for C-V analysis,

lifetime analysis, and Zerbst measurements. These systems permit collection of data pertaining to the mobile ion concentration, interface state traps, lifetime, and surface generation velocity.

The composition and structure of the GaAs surface, the insulating films, and the interface have been analyzed with Auger electron spectroscopy, secondary ion mass spectrometry (SIMS), and transmission electron microscopy (TEM). In the latter case we have developed a new technique for preparing thin vertical sections which permitted direct observation of microstructural features.

III. Characterization Results

(a) Wet Chemical Surface Preparation

We have determined the effect of various wet chemical etchants and the effect of surface treatment with $RuCl_3$ prior to Al_2O_3 deposition have on the interface characteristics using MIS test devices. These results are summarized in Table 1. With the exception of the samples treated with $RuCl_3$, where no capacitance variation could be obtained between ± 20 volts, there are no large differences in the surface generation velocities (V_g) or other characteristics given similar substrate carrier concentrations. SIMS evaluation of an MIS structure after surface preparatin with $RuCl_3$ shows large concentrations of Ru and Cl at the interface. Otherwise, Auger analysis showed the other surface preparations to be approximately equivalent with each leaving a thin contamination layer of C, O, and Cl. We found that the normal surface treatment which we employ prior to liquid phase epitaxial growth (#1 in Table 1) and the NH_4OH treatment (#5 in Table 1) gave the most reproducible results for a number of individual devices measured over a large area wafer. Accordingly we employed these surface treatments prior to *in-situ* etching in future work.

A typical C-V plot and computer printout for an $Al/Al_2O_3/GaAs$ MIS structure which was prepared using surface treatment #1 prior to insulator deposition are shown in Figure 6. The hysteresis near accumulation and the flat band which are normally observed with GaAs MIS devices are present along with a very complicated hysteresis under positive bias which is due to deep depletion. There is also a large shift in the flat band voltage (-12.6 volts). These characteristics are indicative of interface anomalies and traps or mobile ions in the oxide.

A typical Zerbst plot is shown in Figure 7. Surface generation velocities measured on various samples have ranged as low as 600 cm/sec while generation lifetimes have been determined to normally range from 1 to 8×10^{-9} sec for substrate carrier concentrations near 3×10^{16} atoms/cm^3. These lifetime values are typical for GaAs, while the surface generation velocities are unusually low. The surface generation velocities were found to be dependent upon the carrier concentration of the GaAs substrate as shown in Figure 8.

(b) Al_2O_3 Deposition Temperature

The effect of the dielectric deposition temperature upon the interface characteristics has been determined. The temperature was varied between 300°C and 400°C. The results are summarized in Table 2. It can be seen that the deposition temperature has little effect within this range. Hysteresis characteristics of C-V curves for all deposition temperatures were also found to be similar to those shown in Figure 2. Based upon these results, the Al_2O_3 was deposited at 350°C during future work.

(c) Post-Deposition Anneal

In the course of our investigations, we chose to determine the effect of post-deposition annealing temperatures for Al_2O_3 films although this investigation was beyond the scope of the work statement of the contract. The evaluation was especially important since we needed to determine the maximum temperature which could be used for post-dielectric deposition fabrication steps without alteration of the as-deposited interface characteristics. The results of the annealing experiments conducted are shown in Table 3. The carrier concentration of the substrates used for the annealing experiments was 1.5×10^{16} atoms/cm^3. The electrical data indicate that there is little or no change in the interface characteristics for annealing temperatures up to 650°C. However after annealing at 800°C, the surface generation velocity increased drastically and the values of N_B, C min/C max, and τ (lifetime) were altered significantly. This indicates gross interface deterioration after annealing at the higher temperature. We feel that the changes in the electrical characteristics were due to an increase in the donor concentration at the substrate surface and the introduction of surface and bulk traps. This probably resulted from the redistribution of Ga, As, and Al after high-temperature annealing. A comparison of SIMS composition depth profiles for as-deposited samples (350°C) and samples annealed at 800°C indicates the latter to have some Al diffusion into the GaAs. The layers deposited at 350°C also appear to contain some Ga and As, and after annealing at 800°C there is additional enrichment of both Ga and As coupled with the Al diffusion into the GaAs substrate. The SIMS in-depth profile shown in Figure 9 indicate that this is true.

(d) HCl In-situ Etching

We believe that inversion at the Al_2O_3/GaAs interface requires a clean stoichiometric substrate surface prior to oxide deposition and have proposed that an *in-situ* HCl etch process might provide those characteristics. We have attempted to develop this process in the OMCVD system employed for the deposition of Al_2O_3. The controllable parameters of the etch process include the substrate temperature, the HCl flow rate, and the etch time. We have varied these parameters between 22 and 350°C, 10 and 30 cc/min, and 1 and 10 minutes respectively. In the first set of experiments the flow rate was varied between 10 and 30 cc/min in 5 cc/min increments while holding the substrate temperature and etch time constant at 350°C and ten minutes respectively. After subsequent Al_2O_3 deposition, MIS structures were fabricated and evaluated. A comparison of these samples with those which had no in-situ substrate processsing showed that etching sufficient to alter electrical characteristics did not occur at HCl flow rates below 20 cc/min. The initial results were very encouraging with samples in which etching was evident. The 1 MHz C-V plot for a sample cleaned with an HCl flow of 30 cc/min is shown in Figure 10. The hysteresis and stretch out are reduced significntly and the flat band voltage is reduced to -3.8 volts when compared with a normal deposition (Figure 6). These results would indicate a significant reduction in oxide traps or mobile ion charge densities. However, low frequency C-V data showed no indication of inversion, and Zerbst analysis showed that generation velocities for etched samples had increased to 10^7 V/cm while the bulk lifetimes measured were extremely low.

MIS samples were evaluated with SIMS and TEM to understand the anomalies discussed above. SIMS depth profiles are shown for two samples in Figures 11 and 12. Sample MIS-21 was in-situ etched at 350°C for ten minutes with an HCl flow rate of 10 cc/min prior to Al_2O_3 deposition. Sample MIS #22 was etched under identical conditions with the exception that the HCl flow was increased to 30 cc/min. The profiles are similar up to a depth of about 0.6 microns. Beyond 0.6 microns, MIS-21 shows a rapid decrease in oxygen, aluminum, hydrogen, and carbon, and reaches the background level before 1 micron. MIS-22, however, shows a much more gradual decrease in the same elements, reaching the background level at

1.5 microns. Although this can be interpreted as a greater diffusion of these elements into the GaAs substrate, the transmission electron microscopy results give an alternative explanation.

Samples were thinned for transmission electron microscopy using two techniques. Thin vertical cross sections were prepared by carefully cutting strips from the wafer, mounting to expose the cut edges, abrasive polishing, and finally ion micro-milling to obtain a view of the interface between the aluminum oxide and the GaAs substrate. A uniformly thinned section was very difficult to obtain because of the differences in the hardness and chemistry between the GaAs and Al_2O_3. The second technique consisted of cutting a 3 mm disk with an ultrasonic cutter, then etching the GaAs away with bromine in methanol to leave the thin oxide layer intact. Figure 13 shows the vertical cross sections of the two samples. The oxide-GaAs interface is relatively smooth for MIS-21, while MIS-22 shows a protruberance of the oxide into the GaAs. The microstructure seen looking through the layers is shown in Figure 14, where the nature of the protruberances of MIS-22 can be seen more clearly. A stereo pair of micrographs was taken to verify that the features did not actually lie within the oxide layer. They are essentially absent in MIS-21.

During the extensive etching or cleaning of MIS-22, deep channels were apparently formed in the surface of the GaAs. In the subsequent deposition of the aluminum oxide, these were filled with oxide. When the GaAs was later removed with bromine, the oxide retained the morphology of the channels. The channels appear to be about 0.1 microns wide and 1 micron deep. Similar features have been seen in other materials, for example, aluminum foil which is etched and anodized for use in electrolytic capacitors. The channels generally initiate at sites where impurities have concentrated, and then proceed to great depths for reasons that are not clearly understood.

Referring back to the SIMS data for MIS-22, it is now seen that the region between 0.5 and 1.5 microns was inhomogeneous, and contained a mixture of both GaAs and aluminum oxide. MIS-21 had a much more uniform interface, which appeared more abrupt in the depth profile. The penetration depth of the oxide fingers is about 1 micron as measured by both techniques.

The C-V curve of the heavily etched sample (MIS-22) showed less hysteresis, but the surface generation rate was very high. The microstructures may help to explain these electrical results. If there were mobile ions localized in clusters or channels and these were removed by the extensive etching, it would account for the reduction in the hysteresis of the C-V data. However, the microstructural defects introduced at the GaAs surface could increase surface generation velocities and reduce bulk lifetimes.

Further experiments were conducted in an attempt to adjust parameters such that surface oxides and contaminants could be removed without attacking the underlying GaAs substrate. Reduction of the etch temperature to 22°C still gave the poor electrical characteristics discussed above and as the HCl flow was reduced the etch process stopped abruptly near a flow of 20 cc/min. Variation of etch times in this region did not produce the desired results. The onset of substrate attack was coincident with the adverse alteration in the electrical characteristics of MIS structures. We have concluded that HCl etching in an Ar atmosphere with the present system is not a viable process for obtaining a clean stoichiometric GaAs surface.

(e) SiO_2, Si_3N_4, Al_2O_3 Comparison

We have deposited SiO_2 and Si_3N_4 on GaAs to determined the relative merit of these and Al_2O_3 as passivants for GaAs. The GaAs substrates were p-type with a carrier concentration of 7×10^{16} atoms/cm^3.

Silicon nitride films are deposited in a Tegal Plasmaline 100 Reactor by the reaction of either NH_3 or N_2 with silane in an argon carrier, enhanced by an RF plasma generated betweeen two planar electrodes. In this reactor, the sample to be coated is placed on the lower electrode, whose temperature can be controlled anywhere in the range of room temperature to 500°C. Gas flows were maintained by automatic flow controllers; typical flow rates were 50 SCCM of 10% silane in argon, 50 SCCM of either NH_3 or N_2, and 110 SCCM of argon, giving a total ambient pressure of 0.5 Torr. Film properties could be reproducibility varied by adjusting the flow rates and substrate temperature. Films grown at 400°C and above were stoichiometric in the ratio Si_3N_4 with oxygen content below the limits of detectability (<1%), and index of refraction near 2.0. Films grown below 400°C exhibit an index of refraction which decreases uniformly and reproducibility with decreasing substrate temperature to a value of $n=1.65$ for a subsrate temperature of 100°C. This lowering of the index of refraction is indicative of increasing oxygen content, yielding silicon oxynitride $Si_xO_yN_z$. Film uniformity in thickness and composition was excellent over the entire range of substrate temperature and deposition pressures tested, with variations of less than 5% over a 3-inch wafer.

SiO_2 films were deposited in an Applied Materials chemical vapor deposition system using SiH_4 and O_2 in a nitrogen carrier gas. The films typically exhibited an index of refraction between 1.45 and 1.47. The Al_2O_3 films were deposited in the OMCVD system at a temperature of 350°C.

MIS structures were fabricated and evaluated after dielectric deposition. C-V plots at 1 MHz indicated that MIS structures formed with the Al_2O_3 and Si_3N_4 had comparable characteristics while hysteresis and spread out were severe for MIS structures formed with SiO_2. The surface generation velocities for SiO_2, Al_2O_3, and Si_3N_4 were 21,000, 10,000, and 4,000 V/sec respectively. Although the Si_3N_4 exhibited the lowest surface generation velocity, low-frequency C-V data showed no indication of inversion.

(f) MISFET Test Device

Another investigation undertaken which was not proposed in the original contract work statement was that of developing a MISFET fabrication process to evaluate the inversion layer characteristics. We chose to do this since data obtained from C-V and G-V measurements using MIS structures can only give an indication that inversion of the GaAs interface is being achieved but does not provide conclusive evidence. A true test for surface inversion can be obtained by the fabrication and evaluation of an operatinal enhancement mode MISFET device.

A four-level mask set was designed and produced for this purpose. The fabrication steps involved in the process are shown in Figure 15. Initial results obtained from the test wafers processed showed surface generation velocities between 40 and 100×10^3 cm/sec, and the other anomalies noted in the annealing of MIS structures at 800°C were also present. These results indicated that the 800°C implant anneal step produced surface characteristics which could not be reversed by the normal wet etching employed prior to dielectric deposition. Accordingly, development of an alternate fabrication process was initiated employing the same masks. The process steps involved are shown in Figure 16. The major difference from the original process is that the source and drain junctions are formed by an alloy process rather than by an ion-implant followed by a high-temperature anneal for activation. We found that a 400°C five minute anneal of vacuum deposited Au-Ge-Ni gave rasonable junction characteristics. I-V characteristics of the deposition are shown before and after anneal in Figure 17. Since we found no alteration of interface characteristics with the MIS annealing experiments for temperatures up to 650°C, we feel that the problems encountered with the original fabrication process may be alleviated and that MISFET structures fabricated with this process

might be useful for the evaluation of inversion layer characteristics.

SUMMARY

The program objectives outlined in the original contract work statement were completed. We currently feel that we have developed a superior OMCVD process for the deposition of high-quality Al_2O_3. The process can be employed for the deposition of dielectric films on GaAs at sufficiently low temperatures to minimize interface perturbations normally introduced during other deposition methods. We feel that this is the first requirement necessary to obtain inversion of GaAs.

The second requirement is that of obtaining a clean stoichiometric surface prior to dielectric deposition. Our effort to achieve this by the development of an in-situ etching process was unsuccessful. However, the substrate cleaning procedure and insulator deposition process developed by us have resulted in unusually low surface generation velocities.

Although the final goal of inversion at the Al_2O_3/GaAs interface was not achieved, the results from this effort have indicated the direction for future work in this area. Al_2O_3 layers deposited on GaAs using the present process appear to contain some Ga and As. The SIMS in-depth profile shown in Figure 6 indicates that this is true. After annealing at 650°C or 800°C, there is additional enrichment of both Ga and As near the interface. It is reasonable to believe that there is nonstoichiometry at the interface when there is Ga and/or As present in the Al_2O_3 film. This can result in a high density of surface states and prevent inversion the GaAs surface. Similar irregularities have been observed at annealing temperatures in excess of 730°C in the SiO_2/GaAs system (4). More recently H. Hayashi et al. (5) saw this effect at annealing temperatures as low as 400°C. A. Lidow et al. (6) were successful in minimizing similar anomalies by employing a double layer encapsulant consisting of As-doped SiO_2/Si_3N_4, and Hayashi et al. minimized the diffusion of As into SiO_2 by doping the insulator with Ga.

Based upon our results, we would recommend that future work be aimed at the elimination of these anomalies by doping the Al_2O_3 insulator with Ga and/or As. Irregularities which may occur as the result of the deposition process parameters or undesirable surface characteristics should be minimized with this technique. Further, we would recommend that post anneal treatments, preferably in an As ambient, of properly doped Al_2O_3 should be done to promote stoichiometry at the interface. In the latter case, high-temperature anneals will probably be required to promote bonding of elemental Ga and/or As. At high temperatures a competing process of elemental diffusion through grain boundaries and film defects of single-layer insulators might be expected. This problem could be addressed by depositing multilayer insulators of SiO_2 or Si_3N_4 on doped Al_2O_3.

We would also recommend the further development of a MISFET fabrication process and construction of devices to evaluate the inversion layer characteristics. The results of C-V and G-V measurements using MIS structures cannot provide conclusive evidence that inversion of the GaAs surface is being achieved. A true test for surface inversion can be obtained by the fabrication of an operational enhancement mode MISFET device. Employment of this device as a characterization tool will also provide valuable data on the inversion layer charge and mobility which cannot be obtained from tests using MIS structures.

Acknowledgments

W. Katz performed the SIMS analysis for this study. The diligent and careful preparation of the TEM samples, as well as the electron microscopy, was done by E.F. Koch.

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Table 1

SUBSTRATE SURFACE PREPARATION

Final Surface Preparation	Poloron $N_D - N_A$ $\times 10^{16}$ cm^{-3}	C-V N_B $\times 10^{16}$ cm^{-3}	C_{min}/C_{max}	V_g $\times 10^3$ cm/sec	τ $\times 10^{-9}$ sec
1) Oxide, HCl, H_2O, (LPE)	2.5	2.2	0.44	1.0	2.0
	6.0	7.0	0.65	9.0	0.3
2) HCl Boil, MeOH	2.5	2.6	0.46	3.0	2.0
	6.0	7.3	0.68	10.0	0.1
3) Hf, MeOH	2.5	2.4	0.46	2.0	2.0
4) NH_4OH, H_2O	2.5	2.3	0.45	1.9	2.0
5) NH_4OH	2.5	2.4	0.45	3.0	3.0
6) $RuCl_3$	2.5	-	-	-	-

Table 2

EFFECT OF DIELECTRIC DEPOSITION TEMPERATURE ON INTERFACE CHARACTERISTICS

Deposition Temperature (°C)	N_B $\times 10^{16}$ cm^{-3}	C_{min}/C_{max}	V_g $\times 10^3$ cm/sec	τ $\times 10^{-9}$ sec
300	4.5	0.43	8.0	0.7
350	4.3	0.41	4.5	0.7
375	4.5	0.44	6.0	0.6
400	4.4	0.45	7.0	0.7

Table 3

RESULTS OF ANNEALING EXPERIMENTS

Deposition Temperature (°C)	N_B $\times 10^{16}$ cm^{-3}	C_{min}/C_{max}	V_g $\times 10^3$ cm/sec	τ $\times 10^{-9}$ sec
0	1.3	0.49	3.0	3.0
550	1.8	0.45	0.8	7.0
650	1.2	0.47	1.4	7.0
800	0.2	0.70	9.0	0.001

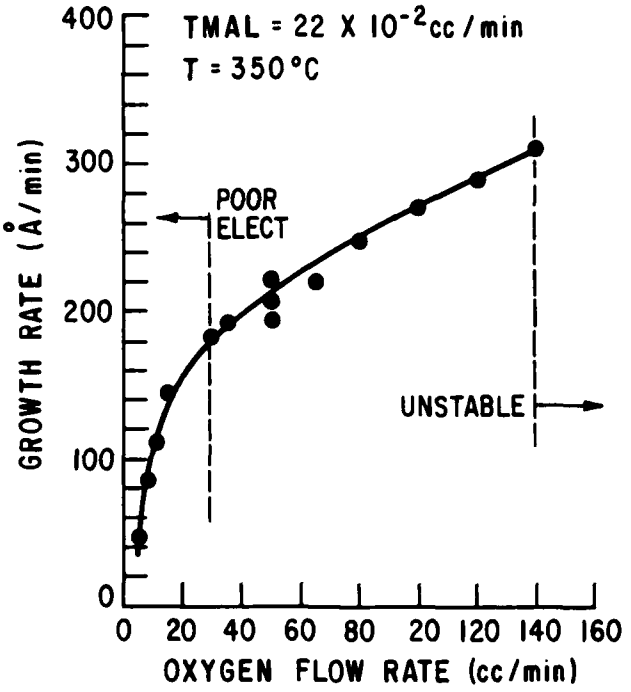


Figure 1. Growth rate vs. oxygen flow rate

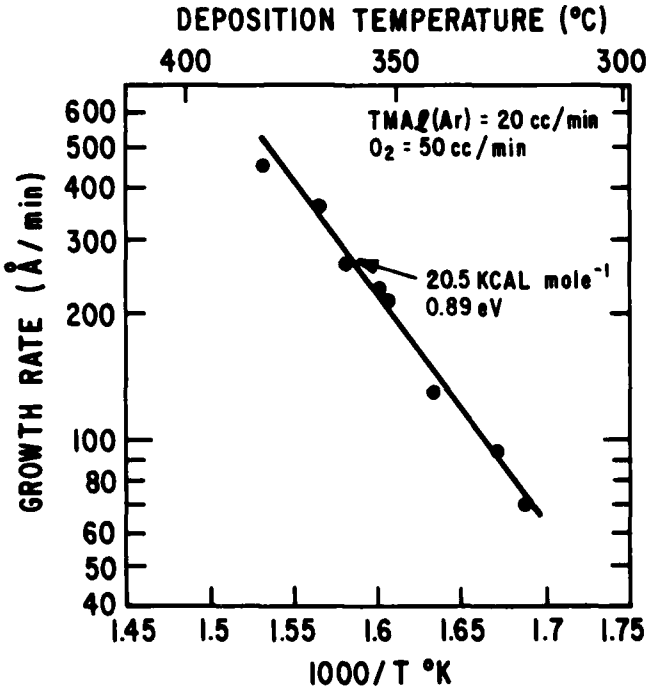


Figure 2. Growth rate vs. deposition temperature

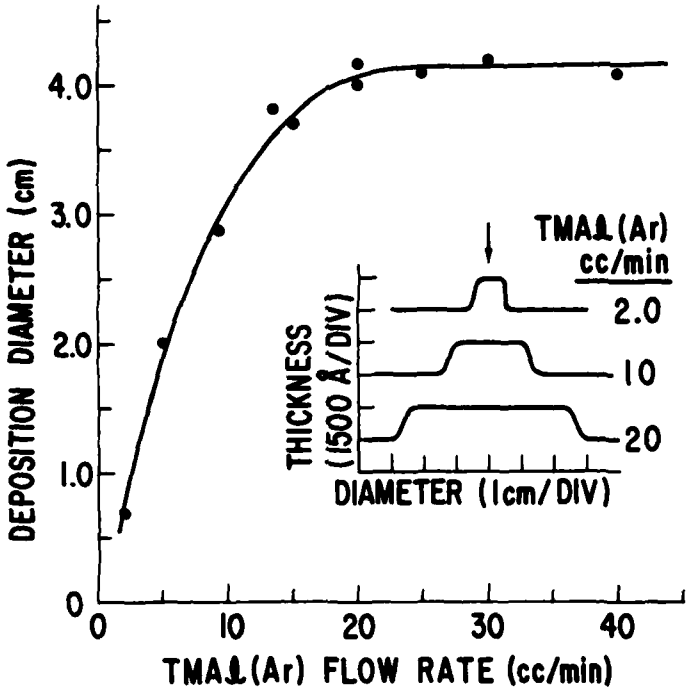


Figure 3. Deposition diameter vs. flow rate

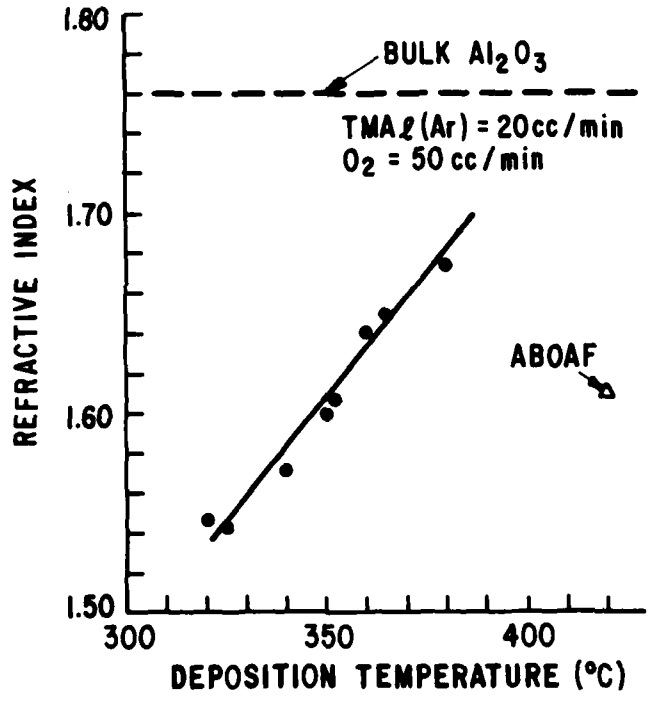


Figure 4. Reactive index vs. deposition temperature

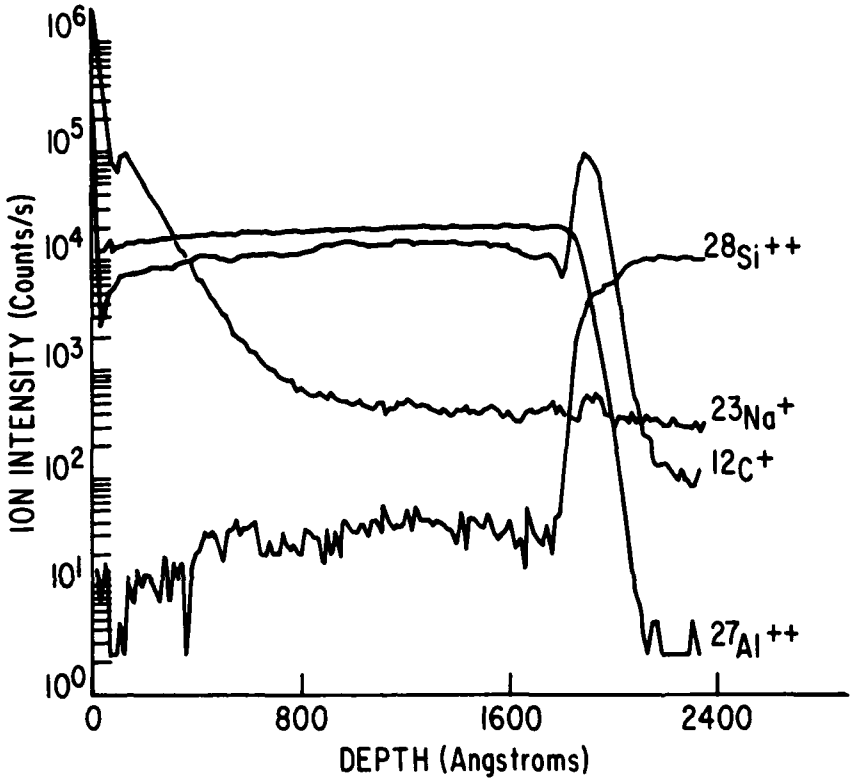
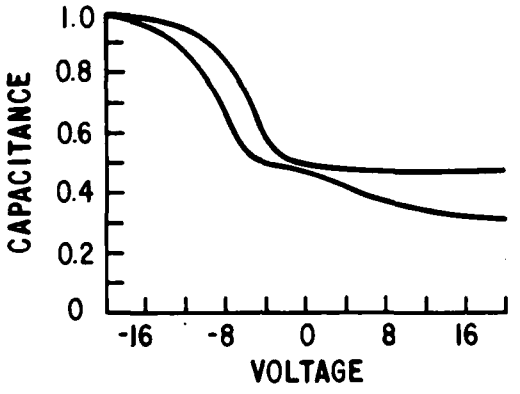


Figure 5. SIMS in-depth profile (Al_2O_3/Si)



CV PLOT	
WAFER ID:	MIS11/C-1
DATE:	4/11/83
MODE:	CAP
WAFER TYPE:	P
RAMP RATE:	1040.0 mv/sec
TOX:	1412.0 A
AREA:	4.90E4 sq μm
CMAX:	24.6 PF
RATIO:	0.465
CFB:	22.0 PF
VFB(1):	-12.6 VOLTS
NB:	2.54E16 cm^{-3}
WMAX	0.266 μm

Figure 6. Typical C-V plots

ZERBST PLOT:	Al_2O_2 #106
WAFER ID:	
DATE:	8/26/82
MODE:	CAP
WAFER TYPE:	P
ACCUMULATION:	-20.0 VOLTS
INITIAL BIAS:	-20.0 VOLTS
DEPLETION:	20 VOLTS
TOX:	1431.9 A
AREA:	4.90E4 sq um
CMAX:	24.2 PF
RATIO:	.45
NB:	1.70E16 cm^{-3}
LIFETIME:	6.67E-10 sec
SURFACE GEN VEL:	612.8 cm/sec
LOWER: 5.03E-2	UPPER: 0.249

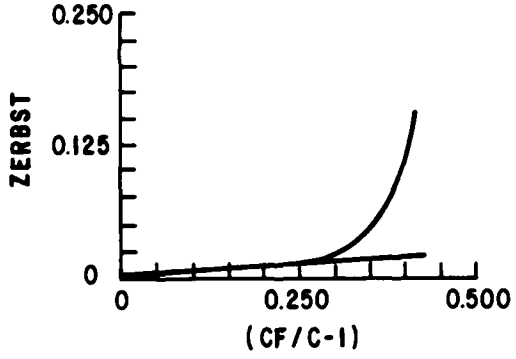


Figure 7. Typical Zerbst plot

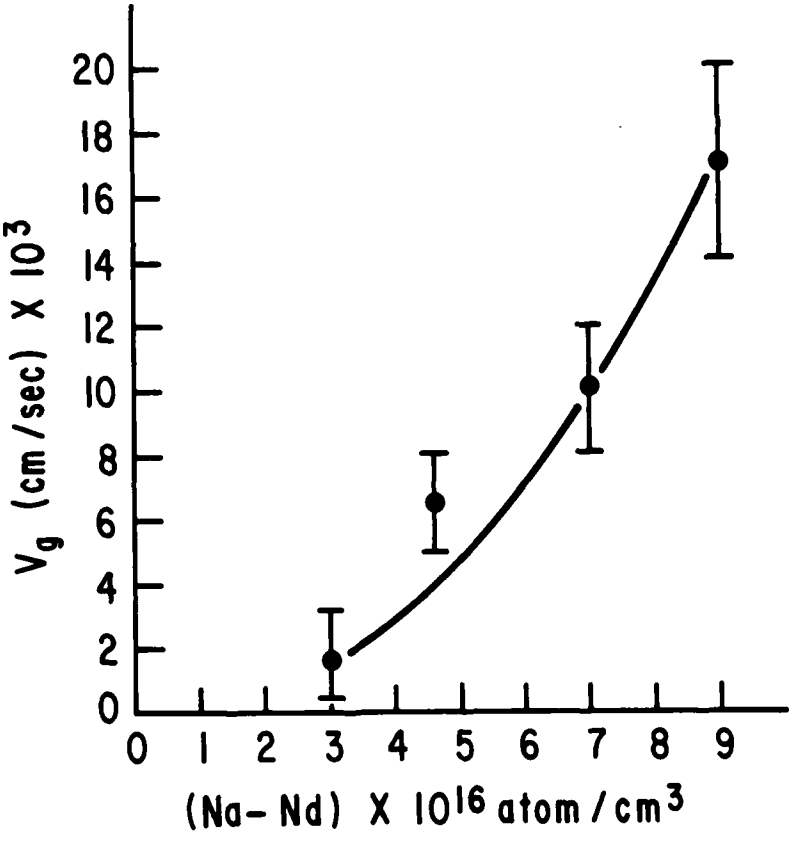


Figure 8. Surface generation velocities vs. concentration of GaAs substrate

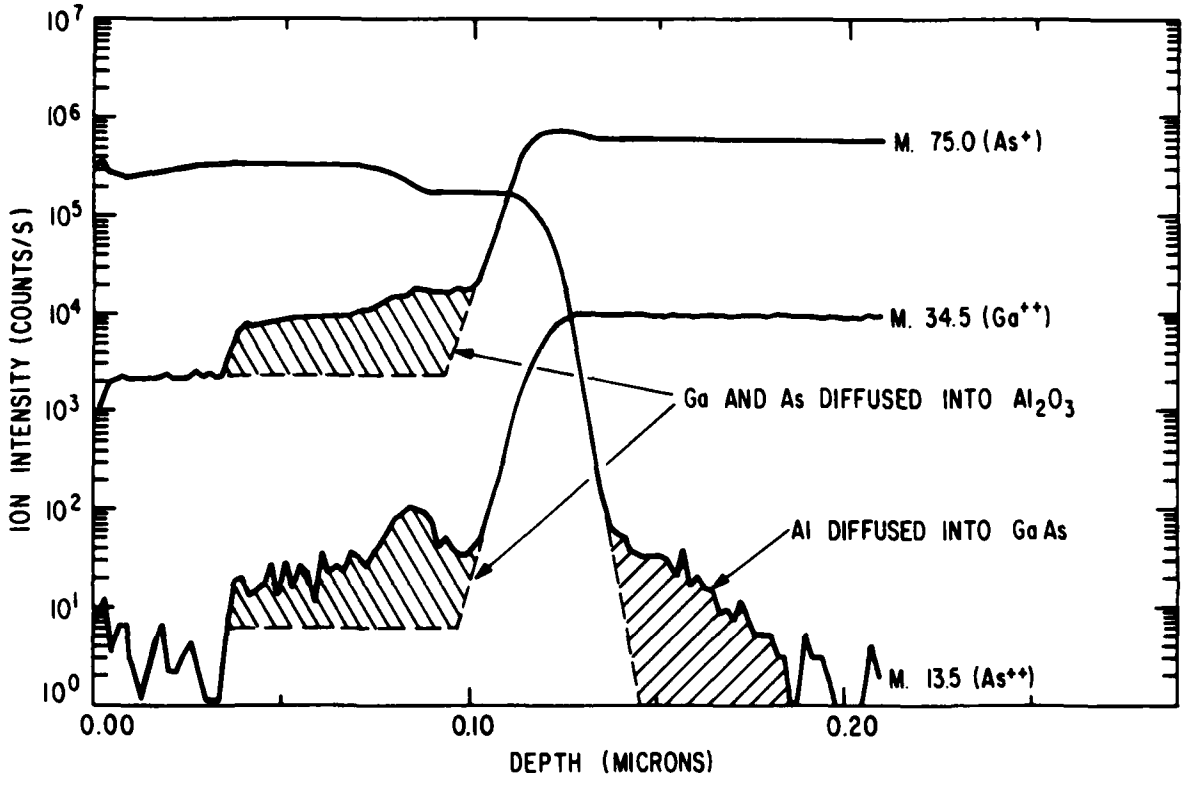


Figure 9. SIMS in-depth profile

WAFER ID:	MIS #22
DATE:	7/6/83
MODE:	CAP
WAFER TYPE:	P
RAMP RATE:	1040.0 mV/sec
TOX:	1289.3 A
AREA:	4.90E4 sq um
CMAX:	26.9 PF
RATIO:	0.589
CFB:	25.2 PF
VFB (1):	-3.83 VOLTS
VT (1):	1.07 VOLTS
NF:	1.19E12 cm^{-2}
NB:	8.68E16 cm^{-3}
WMAX:	0.147um

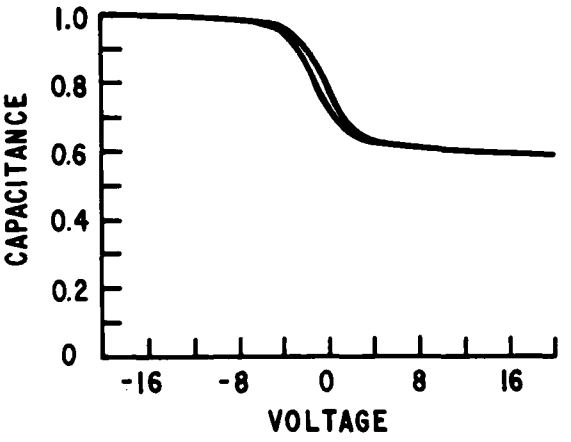


Figure 10. C-V plot for sample cleaned with an HCl flow of 30 cc/min

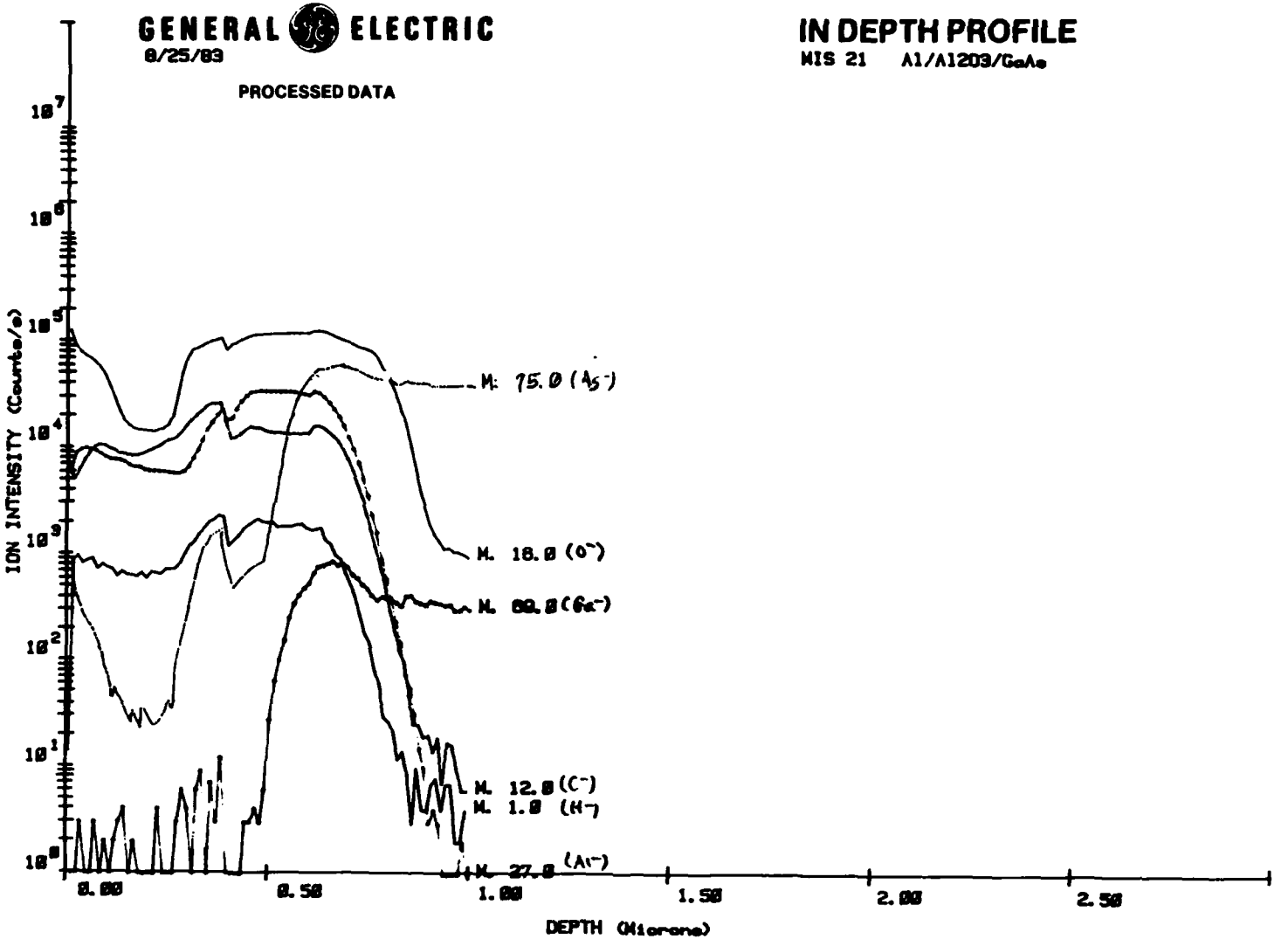


Figure 11. SIMS in-depth profile, MIS 21, HCl−10 cc/min, 350°C, 10 min

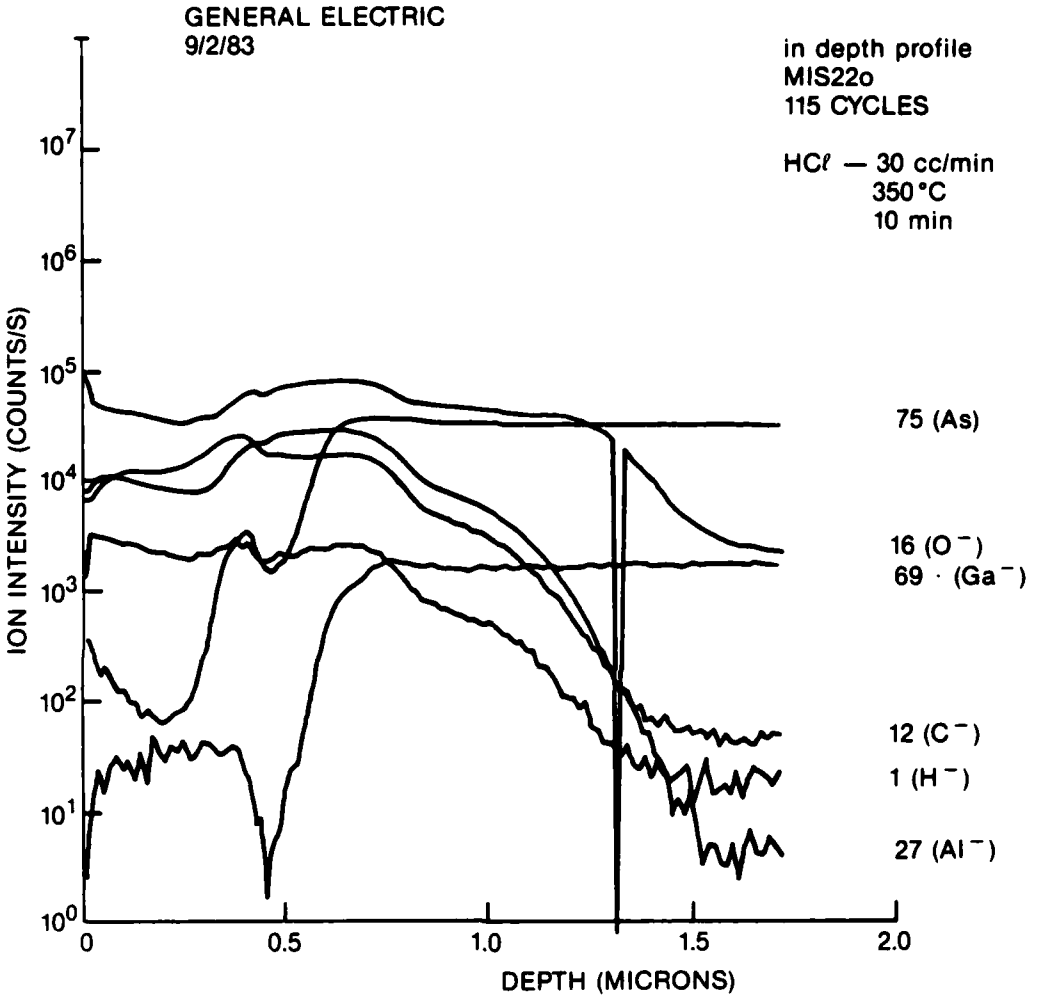


Figure 12. SIMS in-depth profile, MIS 22, HCl−10 cc/min, 350°C, 10 min

Figure 13a. MIS 21, HCl−10 cc/min

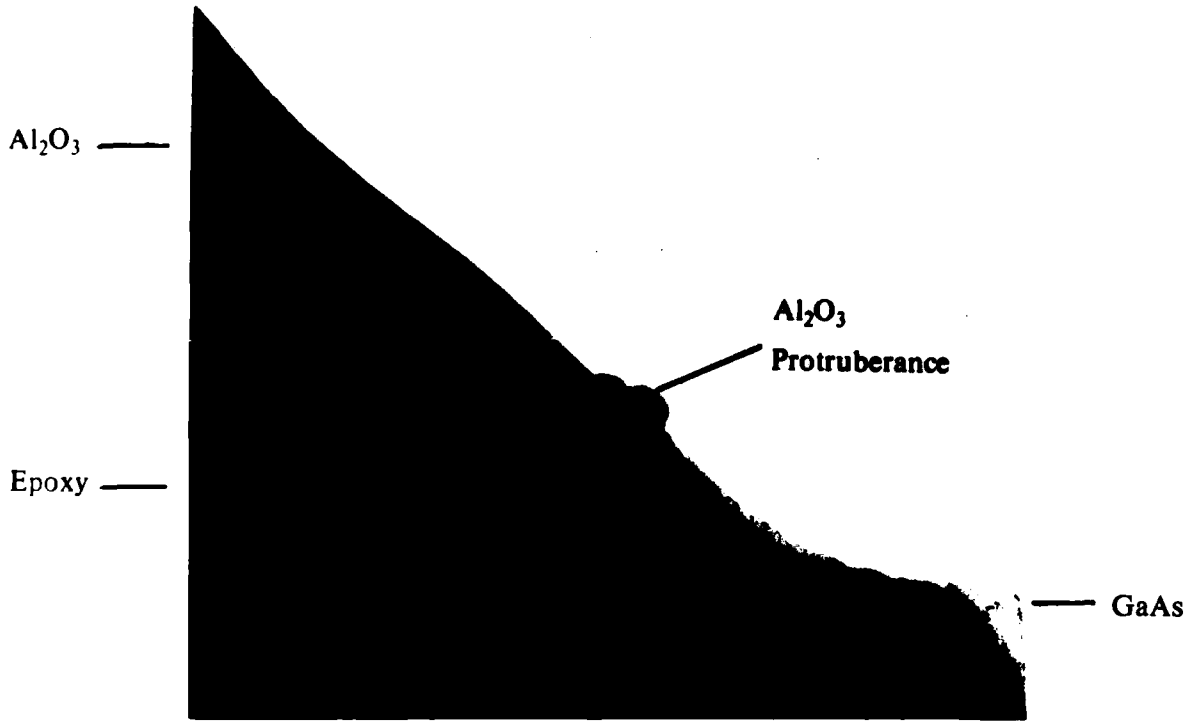


Figure 13b. MIS 22, HCl−30 cc/min

Figure 14a. MIS 21, HCl−10 cc/min

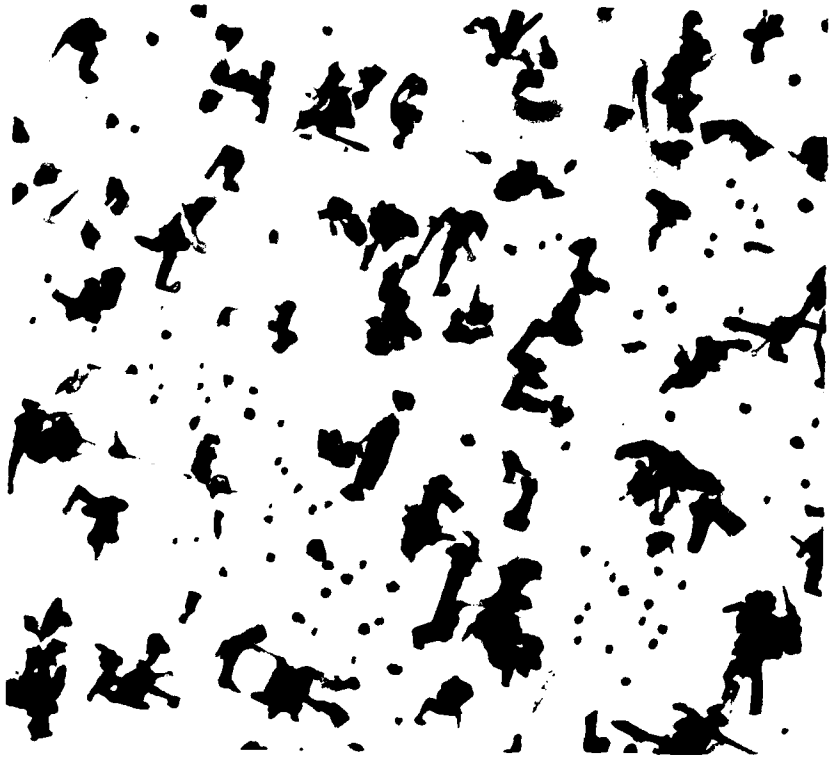


Figure 14b. MIS 22, HCl−30 cc/min

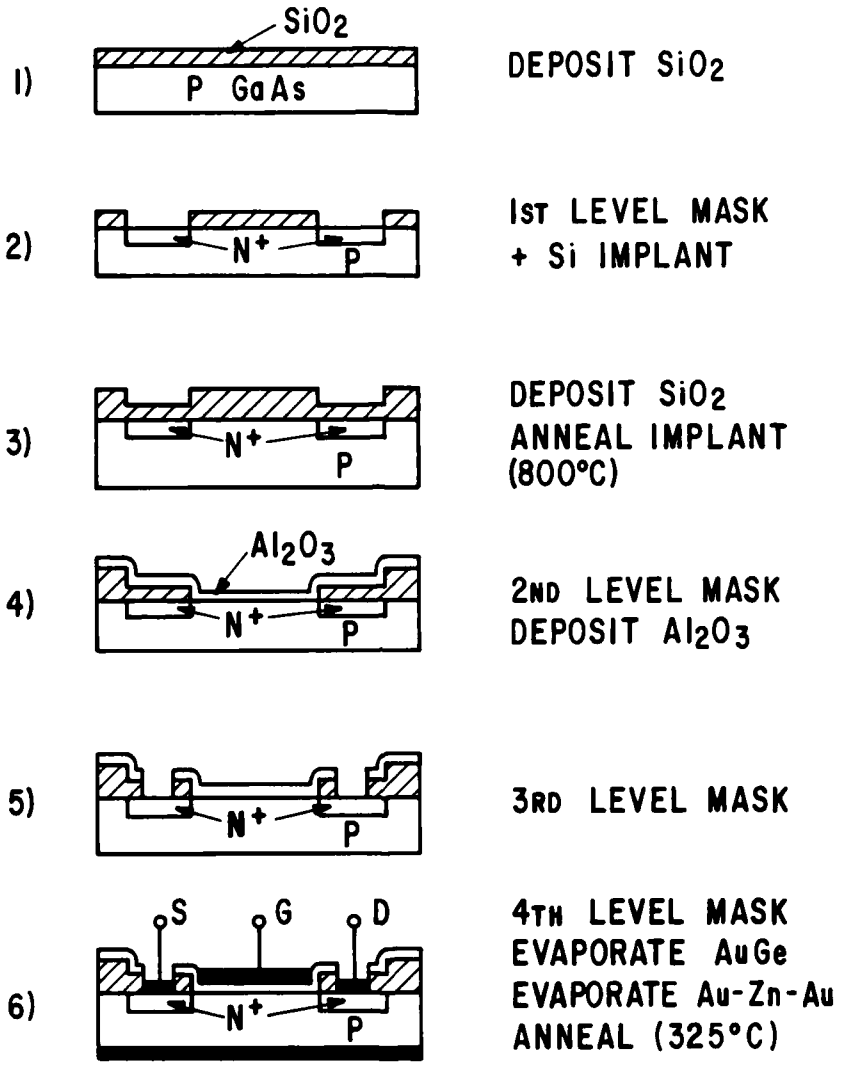


Figure 15. MISFET fabrication process

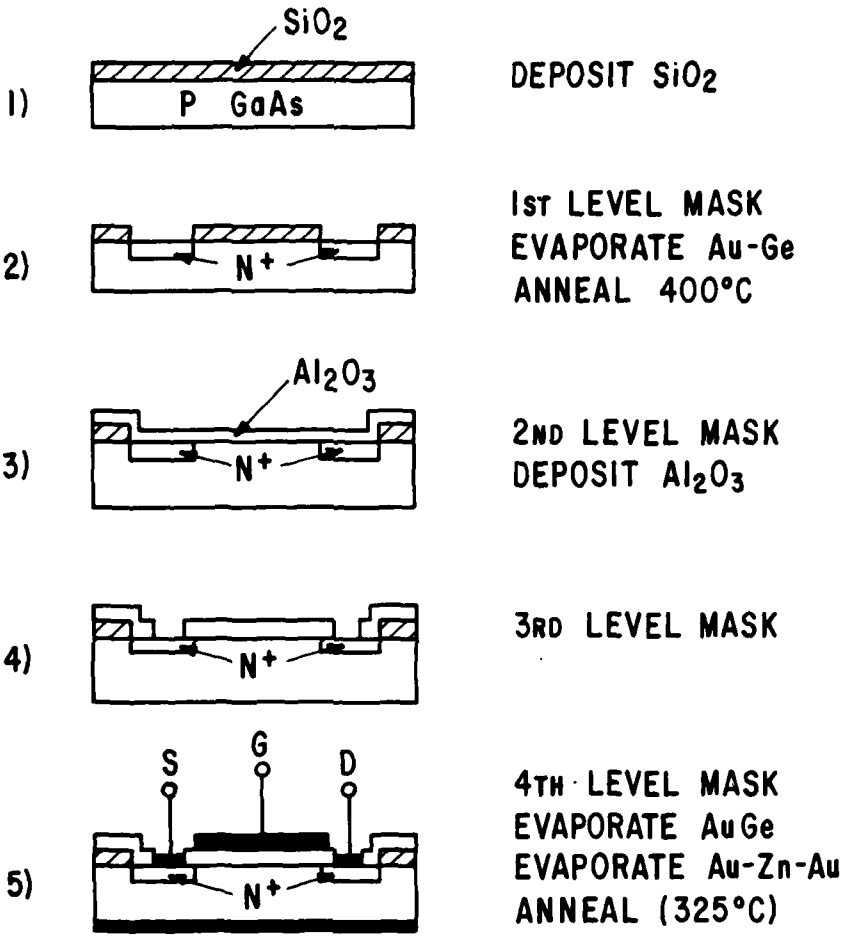


Figure 16. Alternate fabrication process

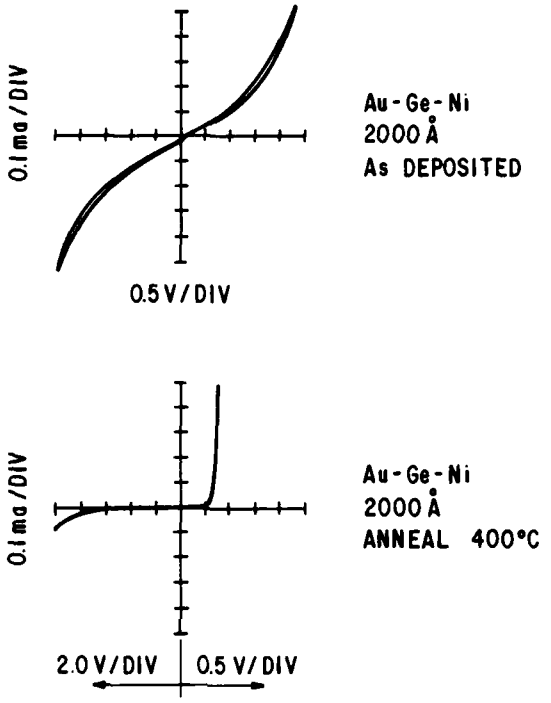


Figure 17. Alloy junction development